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FinFET- Benefits, Drawbacks and Challenges

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Abstract

FinFET is a promising alternative to conventional MOSFET - which has reached its limits and has too much leakage for too little performance gain. FinFET is being recommended as the basis for future IC processes because of its power/performance benefits, scalability, superior controls over short channel effects etc. However, it brings with itself new challenges andundesirable characteristics such as Corner effects, Quantum effects, Width quantization, Layout dependencies, additional parasitics etc. This paper discusses the major advantages, disadvantages and challenges of FinFET technology.

Keywords: FinFET,Dual- Gate,Tri-Gate, Quantum effects, Corner effects, Width quantization, Double Patterning.

Introduction

Conventional MOSFETs have inherent problems of large leakage currents from gate to channel and increasingly unreliable transistor characteristics. To cater these problems, FinFET transistor technology has been developed which has cast a profound impact on the semiconductor industry. Almost all the big players in the semiconductor eco-system are focusing and putting lot of efforts on this promising and disruptive technology. It provides a new pathway for Moore's Law beyond 20nm as they have much better performance and reduced power consumption compared to planar transistors. A 16nm/14nm FinFET process can potentially offer a 40-50% performance increase or a 50% power reduction compared to a 28nm process. The next few years should be very interesting as the benefits of this technology are seen in products from smart phones to servers. Although it has numerous benefits, the move to FinFETs comes with quite a few new challenges such as design-rule complexity and skyrocketing resistance,new Layout Proximity Effects. Routers face difficulty to connect efficiently to pins on standard cells. Furthermore, extracting parasitic from FinFETs is significantly different from regular planar CMOS devices. Thus FinFET processes should be made as transparent and smooth as possible for the designers. To achieve this, Semiconductor industries need to work behind the scenes to ensure that the tools understand and model the complexities involved.

Benefits of Finfet

To exploit different benefits of FinFET, it is fabricated into two types: (1) Dual-gate FinFET, which trims the excess silicon by fabricating the channel using an ultra-thin layer of silicon that sits on top of an insulator, therefore the electric field from the gate to the fin on the top is drastically reduced. (2) Tri-gate FinFET, in which the FET gate wraps around three sides of the transistor's elevated channel, or "fin". Since fins are made vertical in nature, high packing density can be achieved, by packing transistors closer together. Further, to get even more performance and energy-efficiency gains, designers also have the ability to continue growing the height of the fins.

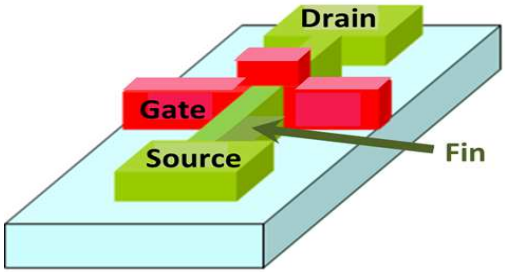

Fig.1 Dual-Gate FinFET Structure

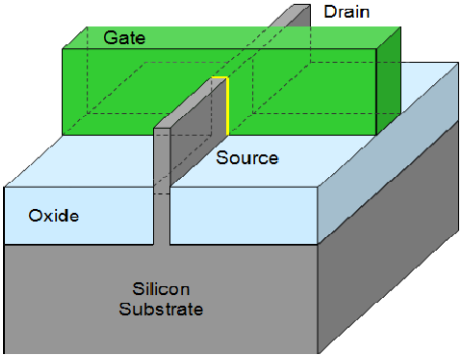

Fig.2 Tri-Gate FinFET Structure

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One important feature of FinFET is the fin thickness, which needs to be smaller than or equal to the gate length. Their scaling does not depend on oxide thickness, which is a big advantage because it's the process lithography that defines the FET characteristics at each new process node. Furthermore, only one extra mask is required to create the silicon fin. Designers also have a choice of extending the width in third dimension in tri gate FinFET without affecting layout area; as a result the effective channel width can be significantly enhanced relative to a planar transistor. The advantage is greater for SRAM layouts, given their dense nature.

It exhibits little or no body effect because FinFET channels are fully depleted. A 4-input FinFET NAND is equivalent to a 3-input planar NAND in terms of delay.

Given the excellent control of the conducting channel by the gate, very little current is allowed to leak through the body when the device is in the off state. The FinFET can also be run at a lower operating voltage for a given leakage current, halving its dynamic power consumption (which is proportional to CV2f) for a 0.7 scaling in VDD.Some of these advantages become more significant as the operating voltage is reduced. At 1V, the FinFET is 18% faster than the equivalent planar device, but at 0.7V, the advantage is 37%. This is attributed to the FinFET's sub-threshold swing (the amount that the threshold voltage has to be changed to halve its leakage) which is lower than in a planar device. This enables the device to be operated at lower threshold voltages for the same leakage. The difference between the gate and threshold voltage at very low operating voltages is much greater, thus exaggerating the performance advantage of very low-voltage FinFETs.

On account of its lower threshold-voltage variability, the channel is well controlled and hence does not need heavy doping, which in turn makes it less susceptible to random dopant fluctuations. Triple gate FinFET has reduced the doping concentration required in the channelto the extent of $10^{15}/cm^3$.Also, Fabrication of FinFET is compatible with that of conventional CMOS, thus making possible very rapid deployment to manufacturing.

Drawbacks and Challenges

Despite the promise of higher performance and better power efficiency, the move to FinFETs comes with quite a few new challenges, For example, the entire tool chain is impacted, including transistor-level process modelling and simulation, mask synthesis, physical extraction, and physical verification, in turn requiring careful re-characterization and validation of models and libraries for higher levels of abstraction and design. One of the goals for the introduction of this fundamental change in process technology is to maintain as much compatibility with previous design flows as possible to enable quick and transparent adoption.

Corner Effects

Though designers have flexibility in variation of height and width of tri-gate, this variationposes different challenges. Although decreasing the fin-width reduces the short channel effects, at the same time the performance of the FinFET may be degradeddue to increase in parasitic drain/source resistance which leads to reduction of drive current and trans-conductance of the device. Moreover, withsmaller fin width, heat cannot flow through easily and device temperature increases. The effect is more pronounced in case of SOI technology, where buried insulating layer causes severe self-heating effects due to low thermal conductivity of oxide layer.

Cross-sectional view of a conventional Tri-gate FinFET is shown in Figure 3. Because of the proximity of gates, the charge sharing occurs in the corner region of the two adjacent gates.This gives rise to premature inversion at the corners.The gate-to-channel electric field is concentrated at the fin corners. As a result, as the gate-to-source input voltage increases toward the device threshold, there will be a higher concentration of sub-threshold leakage current at the corners of the fin, which is known as "corner effect".This premature inversion at the corners of the triple gate FinFET degrades the sub-threshold characteristics of the FinFET which results in higher off state leakage current.

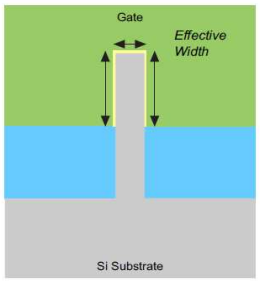

Figure 3Cross-sectional view of conventional Tri-Gate FinFET.

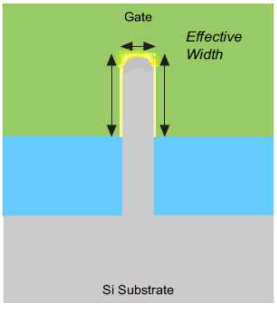

Figure 4 Cross-sectional view of curved Tri-Gate FinFET.

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Recent FinFET's devices in production have a more tapered and rounded profile as shown in Figure 4. In addition to being easier to fabricate, the (sub-threshold) it current crowding effect at the corners is reduced, but introduce additional parasitic extraction challenges.Other techniques available to eliminate the corner effects are reduction in oxide thickness and reduction in doping concentration in channel. It has been observed that sub-threshold leakage current increases for fins with a smaller radius of curvature at the corners.

Fabrication

There are several challenges of FinFET fabrication. Following are the some observations from the recent experiments: (1)The Si surface of fins appears different than in bulk, therefore excessive Si loss was observed after the usual pre-gate-oxide clean. Thus wet cleans are optimized with dilute concentration and lower temperatures. Similarly, the oxidation of fin is also faster at corner and tip of fins.In addition, the dry etching on fins is more stringent due to the 3D structures and a bias plasma pulsing scheme may be viable for minimizing Si loss. (2)As a result of the fin shape, the low-doping in channel is preferred for minimizing sub-thresholdvariations. It also leads to costly implementation of multiple work-functions of gate; fortunately, the multi-V_{cc} scheme can be used for SOC applications.

Extraction of FinFET Parasitics

The 3D nature of FinFETs and the multiple fins pose following challenges:(1) Establish and extend FinFET RC parasitic models to be closer to those extracted using a field solver (2.5D versus 3D). (2) Compact RCs around FinFET not to explode design TATs. (3) Convergence between pre-layout and post-layout by generating good-estimation parasitic RC models ofFinFET.

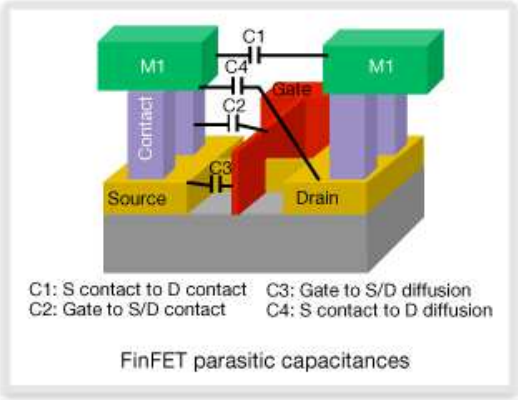

Figure 5FinFET parasitic capacitances.

Figure 5 shows some of the parasitics introduced by this technology. No longer can designers just model transistor length and width - the Registers and Capacitors inside the transistor, including local interconnect, fins, and gates, are critical for predicting the transistor's behaviour. Yet another issue is layer resistance. The 20nm process added a local interconnect layer below the metal 1 layer, and its resistivity distribution is non-uniform and dependent on where the vias are placed. Further, there can be a 100X difference in resistivity between the top metal layers and the lower metal layers. BSIM-CMG is a standard model for FinFETs,but it uses an ideal single-fin model, so it isrequired to multiply thatby the number of fins and fingers, which makes it less accurate.BSIM-CMG model does not yetinclude layout-dependent effects.

Quantum Effects

The FinFET thickness is a key manufacturing parameter. If the FinFET is too thick, the electrostatic influence of the gate on the sides and top of the fin will be weaker, and the fin body will behave more like a (planar device) bulk substrate, losing the benefits of the FinFET topology.

On the other hand, if the FinFET is very thin, then density of available electron (or hole) states is reduced. Under normal circumstances, free electrons/holes have sufficient energy to reside at the conduction/valence energy band edges of the semiconductor material, and therefore conduct current in the transistor channel. The electron/hole energy and band levels in the semiconducting silicon are strong functions of the applied voltages and temperature, which are the basis for the FET model. Normally, there is no shortage of available "free states" for energetic electrons/holes at the band edges. However, for very thin fins, the quantum effect reduces the density of available states at the band edge. As a result, electrons/holes would need more energy to occupy available states higher than the band edge, and be free to conduct device current.

Performance and Variability

Existing FinFETs struggle from a performance and variability perspective: (1) Fin profile shape. A slanted profile is desiredto makes it easy to fill the dielectric between the fins, butthis creates a design that drags down performance and introduces variability. (2) Too few fins can also cause variability. (3) Non-uniform fin doping is another problem which adds to variability.

Width Quantization

As we move to FinFET, one of the challenges is the discrete size of the fin. FinFETs work best as regular structures placed on a grid.So,the transistor width (W), which is one of the main variables for tweaking transistor sizes, is no longer a continuum. Standard cell designers can change the width of a planar transistor, but they cannot change the height or width of a fin, so the best way to increase drive strength is to add more fins. This

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must be done in discrete increments - we can't fins infractions.Channel length variation and body biasing are also limited in value due to the intrinsic characteristics of the FinFET technology.

Double Patterning

There are also challenges that have more to do with the smaller geometries at 16nm and 14nm than FinFETs themselves. One is double patterning(the use of two masks to print alternating features), which is needed at 20nm and below to get features to print correctly with current lithography equipment. It requires extra masks, along with a colorized decomposition process that determines how layout features will be implemented by different masks. Layout-dependent effects (LDE) occur because layout features that are placed near to a cell or device will impact its timing and power. Electro-migration becomes more of a concern as geometries shrink.While double patterning will make immersion lithography practical at 20nm, a new approach will be needed at 10nm.This will be sidewall image transfer (alsocalled self-aligned double patterning) and is much complexthan today's "litho-etch, litho-etch (LELE)"methodology.

Layout dependencies

Layout details have an impact on the stress profile of the FinFET, and hence on its carrier mobility. These details have different effects depending upon whether the fins are situated between two other fins; or are at the end of a row of fins; or are isolated.

Si-Ge depositions in the source and drain areas cut the parasitic resistivity of the source and drain, and create strain that enhances carrier mobility. Fins that are not supported in all directions tend to 'relax' with the strain induced by the Si-Ge lattice mismatch collapsing, reducing the mobility enhancement and leading to a potential significant deterioration of drive current.

Conclusion

FinFETs stand poised to enable the next big leap for computer, communications, and consumer devices of all types.FinFETs have attractive qualities, such asexcellent control of short channel effects, the ability to tune their performance for energy efficiency or performance, which means they can be used as the basis of flexible SoC processes.However, FinFET technology has created new challenges in terms of fabrication processes, corner effects, quantum effects, width quantization, etc. Itrequires a new generation of design experience, expertise, and tools to get the most from the technology.These challenges can be addressed by extensive R&D anddeep collaboration through a Common Platform.

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